PATENT APPLICATION
Docket No. 1482-177

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Barrie Gilbert
Serial No.:	10/766,514
Examiner:	Ryan C. Jager
Filed:	January 27, 2004
Group Art Unit:	2816
For:	SQUARING CELLS AND MULTIPLIERS USING SUMMED EXPONENTIALS
Date:	January 3, 2007

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APPEAL BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal filed October 30, 2006. Appeal is taken from the Examiner's Final Office Action mailed July 31, 2006, and Advisory Action mailed October 19, 2006.

REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Analog Devices, Inc.
One Technology Way
Norwood, MA 02062

RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims canceled: 1-11

Claims rejected: 12-13, 15, 17, 19, 21, 22, 24-26, and 32-36.

Claims allowed: 28-31

Claims objected to: 14, 16, 18, 20, 23 and 27.

Claims appealed: 12-13, 15, 17, 19, 21, 22, 24-26, and 32-36.

STATUS OF AMENDMENTS

Applicant filed a Response to Final Rejection on October 2, 2006 presenting arguments and results of simulations, but no claim amendments. In an Advisory Action mailed October 19, 2006, the Examiner indicated that for purposes of appeal, the amendment would be entered, but Applicant's arguments were not persuasive.

SUMMARY OF CLAIMED SUBJECT MATTER

Claims relating to Sub-Exponential currents

Claim 12 recites a squaring cell having first and second sub-exponential current generators to generate first and second currents in response to an input signal. The current generators are coupled together to combine the first and second currents. An example embodiment of such a squaring cell is illustrated in Fig. 20 and described in the Specification at page 17, line 19 through page 19, line 23. In this embodiment, exponential current generators 52 and 54 generate the two currents I_{C1} and I_{C2} (Specification, page 17, lines 21-23) that are combined at summing node N7 to generate a final output signal I_{SQR} (Specification, page 18, lines 9-10). A sub-exponential current generator is achieved by making resistors $R_S > 0$ in exponential current generators 52 and 54. (Specification, page 19, lines 9-11.) A sub-exponential current generator differs from a true exponential current generator in that it produces a current having an output function that is deliberately "softened" to result in an output that deviates from an ideal exponential function. (Specification, page 19, lines 12-16.) Softening the exponential functions of the current generators may cause the combined output to more closely approximate an ideal square law. (Specification, page 19, lines 16-18.)

Claim 15 recites a method for squaring a signal by generating two currents that vary sub-exponentially responsive to the signal, and combining the first and second currents. This method

may be implemented by the example embodiment illustrated in Fig. 20 and described in the Specification at page 17, line 19 through page 19, line 23. As with claim 12, the use of sub-exponential currents as recited in claim 15 may cause the combined output to more closely approximate an ideal square law. (Specification, page 19, lines 16-18.)

Claim 19 recites a method for squaring a signal by generating first and second currents that vary exponentially responsive to the signal, combining the first and second currents, and altering the first and second currents so as to provide sub-exponential functions. This method may be implemented by the example embodiment illustrated in Fig. 20 and described in the Specification at page 17, line 19 through page 19, line 23. As with claim 12, providing sub-exponential functions as recited in claim 19 may cause the combined output to more closely approximate an ideal square law. (Specification, page 19, lines 16-18.)

Claim 21 recites a multiplier having four sub-exponential current generators for generating first through fourth currents responsive to two input signals. The first and second current generators are coupled together to combine the first and second currents, and the third and fourth current generators are coupled together to combine the third and fourth currents. An example embodiment of such a multiplier is illustrated in Fig. 21 and described in the Specification at page 20, line 32 through page 23, line 10. The operation of the multiplier of Fig. 21 is conceptually similar to the squaring cell of Fig. 20, but instead of using two current generators to provide a simple squaring function, the multiplier of Fig. 21 uses four current generators to provide a full four-quadrant multiplication function. (Specification, page 21, lines 3-7).

In the embodiment of Fig. 21, the current generators may be given a sub-exponential characteristic by using nonzero values for resistors R_S, that is, $R_S > 0$ (Specification, page 22, lines 5-7.) Just as the use of sub-exponential current generators as recited in claim 12 may cause the combined output of a squaring cell to more closely approximate an ideal square law, the use of sub-exponential current generators as recited in claim 21 may cause the output of a multiplier to more closely approximate an ideal multiplication function.

Claim 24 recites a method for multiplying two signals by generating four currents that vary sub-exponentially responsive to the two signals, and combining the first and second currents and the third and fourth currents. This method may be implemented by the example embodiment illustrated in Fig. 21 and described in the Specification at page 20, line 32 through page 23, line

10. As with claim 21, the use of sub-exponential currents as recited in claim 24 may cause the combined output to more closely approximate an ideal multiplication function. (Specification, page 22, lines 5-7.)

Claims relating to Scaling Currents in operation

Claim 17 recites a method for squaring a signal by generating first and second currents that vary exponentially responsive to the signal, and combining the first and second currents. Claim 17 further recites scaling the first and second currents responsive to a control signal while generating and combining the first and second currents. This method may be implemented by the example embodiment illustrated in Fig. 20 and described in the Specification at page 17, line 19 through page 19, line 23. The scaling function maybe implemented by varying the currents I_0 shown in Fig. 20 as described in the Specification at page 20, lines 24-27.

Unlike claim 15, claim 17 is not limited to currents that vary sub-exponentially. Thus, in the example embodiment of Fig. 20, the resistors R_S may be omitted ($R_S = 0$). However, claim 17 recites scaling the first and second currents responsive to a control signal while generating and combining the first and second currents. In other words, the scaling is performed while the circuit is in operation. As disclosed in the Specification at page 20, lines 25-28 scaling the first and second currents while the circuit is in operation may provide the benefit of allowing squaring and weighting functions to be performed simultaneously, e.g., by using a weighting signal as the control signal.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 12-13, 15, 19, 21-22 and 24-25 are unpatentable under 35 USC 102(e) as being anticipated by U.S. Patent No. 5,909,136 to Kimura ("Kimura").

Whether claims 17 and 26 are unpatentable under 35 USC 103(a) as being obvious in view of the combination of U.S. Patent No. 5,909,136 to Kimura ("Kimura") and U.S. Patent No. 6,173,346 to Wallach et al. ("Wallach").

ARGUMENT

Claims Rejections Under 35 U.S.C. §102

Claims 12-13, 15, 19, 21-22, 24-25 and 32-36 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,909,136 issued to Kimura ("Kimura"). Applicant traverses this rejection.

Claim 12

A prior technique for achieving a square-law function involves the use of two opposing exponential current generators that are arranged so that their currents are combined to produce a single output current that obeys an approximate square-law. This is graphically illustrated in Fig. 3 of Kimura which shows how the output I_{D3} from a first exponential current generator and the output I_{D2} from a second exponential current generator may be summed to produce a final output I_{SQ} that approximates a square-law.

Claim 12 recites a squaring cell having two sub-exponential current generators. A sub-exponential current generator differs from a true exponential current generator in that it produces a current having an output function that is deliberately "softened" to result in an output that deviates from an ideal exponential function. (Specification, page 19, lines 12-16.) Purposely softening the exponential functions of the current generators may cause the combined output to more closely approximate an ideal square law. (Specification, page 19, lines 16-18.) In other words, combining two *true* exponential functions produces an inaccurate square-law, but combining two *sub*-exponential functions may produce a more accurate square-law.

An embodiment of squaring cell having sub-exponential current generators is shown in Fig. 20 of the present application. In the absence of the two resistors R_S in Fig. 20, the current generators 52 and 54 would be true exponential current generators due to the exponential characteristic of the transistors as explained in the Specification at page 17, line 30 through page 18, line 8. The inclusion of resistors R_S, however, alters the outputs I_{C1} and I_{C2} so as to soften the shape of the exponential functions, thereby providing a better approximation of a true square-law as described in the Specification at page 19, lines 5-7.

In the Office Action dated February 7, 2006 (paper no. 020406), the Examiner argues that Kimura discloses sub-exponential current generators because the exponential function set forth in

equation 17 (col. 8, line 18) is based on an approximation. Specifically, the Examiner points to Kimura's assumption, while deriving equation 17, that the DC common-base current gain factor α_F for a transistor is equal to 1, when in practice, α_F is typically equal to 0.98-0.99 for a transistor made with ordinary semiconductor device manufacturing processes. (Col. 8, lines 3-6.)

However, the Examiner has failed to show how, if at all, this approximation affects the exponential relationship. There is no argument or evidence as to whether an α_F that is not equal to one would soften the exponential function (which *would* create a sub-exponential function), sharpen the exponential function (which would create something that might be deemed a super-exponential function rather than sub-exponential), have some other effect, or have no effect at all.

In essence, the Examiner is arguing that Kimura inherently discloses a sub-exponential current generator. But in relying upon a theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (BPAI 1990). Since the Examiner has not shown how a sub-exponential current generator necessarily flows from the teachings of Kimura, the rejection of claim 12 is not properly supported.

In response to Applicant's arguments, the Examiner alleged in the Final Office Action dated July 31, 2006 (paper no. 20060719), that $I_C = \alpha_F * I_E$, and therefore, the current at the emitters of Q9 and Q14 must be softened because α_F is always less then 1 in a real transistor, and therefore, I_C is always less than I_E.

However, the fact that I_C is always less than I_E does not say anything about the shape of the output function, i.e., whether the exponential function is softened or not. That is, the Examiner has failed to show how the fact that αF is always less then 1 in a real transistor necessarily leads to the conclusion that it would soften the exponential function to create a sub-exponential function as recited in claim 12.

This failure of proof is enough to justify reversal of the rejection of claim 12. Nonetheless, in the Response to Final Rejection filed October 2, 2006, Applicant provided the following analysis of Kimura's teachings as they would be understood by one of ordinary skill in the art.

Kimura, in Fig. 5, discloses a squaring circuit using bipolar transistors (column 6, lines 54-57). The circuit has two differential pairs of transistors, Q1-Q2 and Q3-Q4. The

differential output ΔIc of the first differential pair Q1-Q2 is given by equation 14. Also, equations 15 and 16 set forth the relationship between different currents in the differential pair. Kimura states that if the DC common base current gain α_F =1, then equations 14, 15 and 16 may be combined to obtain equation 17, which discloses an exponential current generator. However, Kimura further states that α_F may in practice be in the range of 0.98-0.99. To better understand the effects of α_F on I_{C2}, Kimura's equations 15 and 16 may be substituted into equation 14, and the well-known relationship $\tanh(x) = \frac{\exp^x - \exp^x}{\exp^x + \exp^x} = \frac{\exp^{2x} - 1}{\exp^{2x} + 1}$ may be used to obtain:

$$I_0 - Ic_2 = \alpha_F (I_0 + Ic_2) \frac{\exp^{2\frac{V_i}{2V_T}} - 1}{\exp^{2\frac{V_i}{2V_T}} + 1} \qquad \text{Eq. A}$$

which may be rearranged as follows:

$$I_0 \left(1 - \alpha_F \frac{\exp^{\frac{V_i}{V_T}} - 1}{\exp^{\frac{V_i}{V_T}} + 1} \right) = Ic_2 \left(1 + \alpha_F \frac{\exp^{\frac{V_i}{V_T}} - 1}{\exp^{\frac{V_i}{V_T}} + 1} \right) \qquad \text{Eq. B}$$

$$Ic_2 \left(\exp^{\frac{Vi}{V_T}} + 1 + \alpha_F \left(\exp^{\frac{V_i}{V_T}} - 1 \right) \right) = I_0 \left(\exp^{\frac{V_i}{V_T}} + 1 - \alpha_F \left(\exp^{\frac{V_i}{V_T}} - 1 \right) \right) \qquad \text{Eq. C}$$

$$Ic_2 = I_o \frac{\exp^{\frac{V_i}{V_T}} + 1 - \alpha_F \left(\exp^{\frac{V_i}{V_T}} - 1 \right)}{\exp^{\frac{V_i}{V_T}} + 1 + \alpha_F \left(\exp^{\frac{V_i}{V_T}} - 1 \right)} \qquad \text{Eq. D}$$

Equation D illustrates how Kimura's I_{C2} is related to α_F. For α_F =1, the above equation is equivalent to equation 17 of Kimura, which is a pure exponential function. However, for other values of α_F, the behavior of I_{C2} deviates from a pure exponential function as shown in the following table which is included in the Evidence Appendix and reproduced here for convenience. The table illustrates the output I_{C2} for various values of input voltage Vi for three different values of α_F (0.98, 0.99 and 1). A normalized value of I_0 =1 is assumed.

Vi / V_T	Ic2 (for α_F = 0.98)	Ic2 (for α_F = 0.99)	Ic2 (for α_F = 1.0)
0	1	1	1
0.25	0.782744	0.78077	0.778801
0.5	0.612877	0.609697	0.606531
0.75	0.480176	0.476261	0.472367
1	0.376581	0.372216	0.367879
1.25	0.29575	0.291111	0.286505
1.5	0.232707	0.2279	0.22313
1.75	0.183553	0.178643	0.173774
2	0.145238	0.140265	0.135335
2.25	0.115377	0.110366	0.105399
2.5	0.09211	0.087074	0.082085
2.75	0.073981	0.068931	0.063928
3	0.059858	0.054798	0.049787
3.25	0.048856	0.043791	0.038774

From the table it is apparent that as Vi/V_T increases, the value of the current I_{C2} increases more rapidly when $\alpha_F = 0.99$ (or $\alpha_F = 0.98$), than when $\alpha_F = 1$. Thus, for $\alpha_F < 1.0$, the current I_{C2} exhibits a steeper slope that sharpens the exponential function, i.e., it exhibits what can be described as a ***super***-exponential function rather than a ***sub***-exponential function as recited in claim 1.

In the Advisory Action dated October 19, 2006, the Examiner rejected Applicant's reasoning and argued that, even though claim 12 recites a sub-exponential current generator, it does not explicitly require the generated currents to be sub-exponential. Although Applicant acknowledges that claims are to be given their broadest reasonable interpretation during prosecution, the Examiner's proposed interpretation is unreasonably broad. The meaning of "sub-exponential" is abundantly clear from the Specification, and in view of the amendments and arguments presented by Applicant, a person of ordinary skill in the art would understand that a sub-exponential current generator as recited in claim 12 would generate currents that conform to a sub-exponential characteristic.

Claims 15, 19 and 24

For the most part, Applicant argues these claims as a group with claim 12. However, in the Advisory Action dated October 19, 2006, the Examiner commented that, regarding claims 15,

19 and 24, the collector current of a transistor follows a substantially exponential path, but since the gain factor of the transistor is less than 1, the actual collector current is less than the exponential curve used to model it. As best understood by Applicant, the Examiner is arguing that Applicant's table of values is incorrect because the gain factor α_F is always less then 1 in a real transistor. However, Applicant's table of values explicitly models the output current I_{C2} for $\alpha_F = 0.99$ and $\alpha_F = 0.98$, which according to Kimura, are typical values for a real transistor (col. 8, lines 1-6).

Claims 13, 21-22, 25 and 32-36

For purposes of this appeal, Applicant argues these claims as a group with claim 12.

Claims Rejections Under 35 U.S.C. §103

Claims 17 and 26 are rejected under 35 U.S.C. §102(a) as being unpatentable over Kimura in view of U.S. Patent No. 6,173,346 issued to Wallach, et al. ("Wallach"). Applicant traverses this rejection.

Claim 17

Claim 17 recites scaling the first and second currents while generating and combining the first and second currents. In other words, the scaling is performed while the circuit is in operation. In the embodiment of Fig. 20, scaling may be accomplished by varying the bias currents I_0 in response to a control signal as explained in the Specification at page 20, lines 24-27. The specification further discloses at page 20, lines 25-28 that scaling the first and second currents while the circuit is in operation may provide the benefit of allowing squaring and weighting functions to be performed simultaneously, e.g., by using a weighting signal as the control signal.

Kimura discloses varying certain bias signals by programming them in a manner that would have the effect of scaling the first and second currents (col. 8, lines 57-58). However, the Examiner acknowledges that Kimura does not disclose scaling the bias signals while the circuit is in operation. Kimura only mentions that programming the bias signals allows for easy circuit design and integration in large scale integration (LSI) (col. 8, lines 58-62).

From this, the Examiner makes the analytical leap, in the Office Action dated February 7, 2006 (paper no. 020406), that it would have been obvious to perform the scaling operation while the circuit is in operation because it would be desirable to do so because the circuit does not need to be powered down. In support of this leap, the Examiner cites Wallach as teaching the desirability of adding or replacing the functionality of a circuit using programming without powering down the system. There are several problems with this argument.

First, Wallach is not pertinent art. Claim 17 recites a method which, in view of the specification, is directed to the realm of analog signal processing. The specification discusses numerous embodiments of transistor-level circuits in terms of signals, currents, squaring, multiplying, etc., as analog concepts. In contrast, Wallach relates to "I/O adaptors in computer systems" (col. 5, lines 40-41) which are digital systems. Thus, Wallach would not be considered reasonably pertinent to the particular problem with which the inventor was involved.

Second, as best understood by Applicant, the Examiner's arguments regarding not needing to "power down the system" seem to contemplate a notion of discrete operating modes where the system switches between different fixed operating parameters. However, as disclosed in Applicant's specification, scaling the currents while the circuit is in operation may enable not just a change in modes, but rather the integration of two functions into one operation, e.g., allowing squaring and weighting functions to be performed simultaneously. None of the cited references provide the suggestion or motivation for such a modification to the prior art.

Third, claim 17 recites scaling the first and second currents responsive to a control signal. In one embodiment, such a control signal may be a weighting signal as discussed above. The examiner alleges that Kimura discloses a current source I_0 that can be scaled in response to a control signal, but identifies no such control signal, nor any suggestion or motivation to scale anything in response to a control signal. Kimura teaches that I_0 is a constant current source (col. 8, line 23), and at most may be a programmable parameter (col. 8, line 59) which allows easy circuit design and is suitable for LSI. But these teachings relate to varying parameters at the time the circuit is designed and manufactured, not while it is operating, and not in response to a control signal.

Finally, not only is the combination of Kimura and Wallach untenable, but it is based on an impermissible hindsight reconstruction using the Applicant's disclosure as a roadmap to achieve the claimed invention. The Examiner has not identified any motivation or suggestion in

Kimura, Wallach, or any other reference, to scale sub-exponential currents while the circuit is in operation. Thus, a *prima facie* case of obviousness has not been established for claim 17.

In the Final Office Action dated July 31, 2006 (paper no. 20060719), the Examiner advanced the following arguments. Regarding Applicant's (first) argument that Wallach is not pertinent art, the Examiner responded that Wallach relates to electronic circuits and is therefore pertinent. However, "electronic circuits" is an overbroad characterization of the subject matter. In evaluating whether a reference is reasonably pertinent to the particular problem with which the inventor was involved, the structure and function of the claimed subject matter should be compared to that of the reference. Claim 17 recites generating currents, and its function is to provide the mathematical square of two analog signals. Wallach does not disclose any electrical currents, and the function of Wallach's technology relates to hot-swapping I/O adaptors in computer systems. Wallach does not disclose the manipulation of any analog signal, much less the squaring of an analog signal as recited in claim 17. Thus, the structure and function of Wallach is so different from that of claim 17, that Wallach cannot be considered reasonably pertinent.

The Examiner tried to characterize the problem as modifying a circuit *parameter* while in operation. But the method recited in claim 17 does not just modify a parameter, it enables an entirely new mode of operation and additional functionality by allowing a squaring cell to perform squaring and weighting functions simultaneously, in response to a control signal that operates as an additional input, as disclosed in the specification at page 20, lines 25-28. Wallach discloses no such functionality that a person of ordinary skill in the art would have turned to for guidance.

Regarding Applicant's (second) argument that the method recited in claim 17 enables squaring and weighting functions to be performed simultaneously, the Examiner argued that this benefit is not recited in the claim. However, the Examiner has not cited, and Applicant is unaware of, any authority for the proposition that a potentially beneficial result must be recited in the claim.

Regarding Applicant's (third) argument that Wallach does not identify a control signal and only teaches changing parameters during design or manufacture, the Examiner responded that (1) parameters that are applied during design or manufacture would be called design parameters, and (2) electrically programmable parameters read to an electrical signal. As best

understood by Applicant, the essence of this argument is that, if something can be programmed, then it can be programmed in response to a signal. But this still fails to identify all of the elements of claim 17 in the cited references, as well as any motivation or suggestion to modify or combine the references.

Regarding Applicant's (fourth or final) argument that the combination of Kimura and Wallach is untenable and based on an impermissible hindsight reconstruction, the Examiner responded that Wallach teaches adjustment of a circuit while in operation, and Kimura teaches adjusting exponential currents in general. According to the Examiner's logic, if something can be adjusted, then it would be obvious to adjust it during operation. This is an unreasonably broad interpretation of Wallach, and it ignores the rule that a claim must be interpreted as a whole. Claim 17 recites a method for squaring a signal by generating and combining two currents, and simultaneously scaling the currents in response to a control signal. Simultaneously scaling the currents in response to a control signal does not "adjust" a circuit as alleged by the Examiner, it enables an entirely new mode of operation and additional functionality by allowing a squaring cell to perform squaring and weighting functions simultaneously, where the control signal serves as an additional input, as discussed above.

In the Advisory Action dated October 19, 2006, the Examiner responded to Applicant's arguments as follows. Regarding Applicant's first argument that Wallach is not pertinent art, the Examiner responded that Wallach teaches that a circuit can be adjusted during operation, and the Examiner believes this is more than enough for one or ordinary skill in the art to consider adjustment during operation. This is nothing more than a conclusory allegation and falls far short of the fact-intensive comparison of the claimed invention with the prior art required by section 103. *In re Ochiai*, 37 USPQ2d 1127, 1132 (Fed. Cir. 1995).

Regarding Applicant's argument that Wallach discloses no such functionality (performing squaring and weighting functions simultaneously) that a person of ordinary skill in the art would have turned to for guidance, the Examiner responded that such a feature is obviously advantageous to every circuit that needs adjustment that has ever been invented. But this is just circular reasoning to conclude that the claimed invention would have been obvious because it is obviously advantageous.

The Examiner concluded the Advisory Action with arguments to the effect that, if simultaneous scaling and weighting operations are to be given patentable weight, then they must

be recited in the claims. But simultaneous scaling is a limitation of claim 17. Claim 17 recites "scaling the first and second currents responsive to a control signal *while* generating and combining the first and second currents." The Examiner and Board may take official notice of the fact that the word "while" means "at the same time", i.e., simultaneous.

Claim 26

For purposes of this appeal, Applicant argues claim 26 as a group with claim 17.

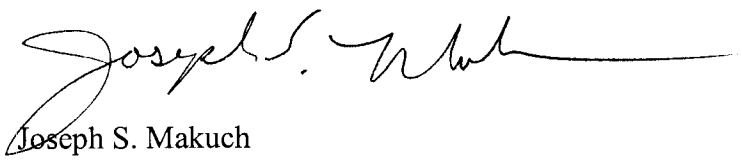
CONCLUSION

Applicant requests that the rejection of claims 12-13, 15, 17, 19, 21, 22, 24-26, and 32-36 be reversed.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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CLAIMS APPENDIX

The following claims are involved in the appeal:

12. (Rejected) A squaring cell comprising:

a first sub-exponential current generator for generating a first current responsive to an input signal; and

a second sub-exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents.

13. (Rejected) A squaring cell according to claim 12 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

15. (Rejected) A method for squaring a signal comprising:

generating a first current which varies sub-exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies sub-exponentially responsive to the signal such that the second current decreases when the signal increases; and

combining the first and second currents.

17. (Rejected) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

scaling the first and second currents responsive to a control signal while generating and combining the first and second currents.

19. (Rejected) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

altering the first and second currents so as to provide sub-exponential functions.

21. (Rejected) A multiplier comprising:

a first sub-exponential current generator for generating a first current responsive to a first input signal and a second input signal;

a second sub-exponential current generator for generating a second current responsive to a third input signal and a fourth input signal;

a third sub-exponential current generator for generating a third current responsive to the first input signal and the fourth input signal; and

a fourth sub-exponential current generator for generating a fourth current responsive to the third input signal and the second input signal;

wherein the first and second sub-exponential current generators are coupled together to combine the first and second currents; and

wherein the third and fourth sub-exponential current generators are coupled together to combine the third and fourth currents.

22. (Rejected) A multiplier according to claim 21 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

24. (Rejected) A method for multiplying a first signal and a second signal, wherein the first input signal is the difference between a first signal and a third signal, and the second input signal is the difference between a second signal and a fourth signal, the method comprising:

generating a first current which varies sub-exponentially responsive to the first signal and the second signal;

generating a second current which varies sub-exponentially responsive to the third signal and the fourth signal;

generating a third current which varies sub-exponentially responsive to the fourth signal and the first signal;

generating a fourth current which varies sub-exponentially responsive to the second signal and the third signal;

combining the first and second currents; and

combining the third and fourth currents.

25. (Rejected) A method according to claim 24 wherein:

combining the first and second currents includes summing the first and second currents; and

combining the third and fourth currents includes summing the third and fourth currents.

26. (Rejected) A method according to claim 24 further including scaling the first, second, third, and fourth currents responsive to a control signal while generating and combining the currents.

32. (Rejected) A squaring cell according to claim 12 wherein the first and second currents comprise substantially sub-exponential currents.

33. (Rejected) A method according to claim 17 wherein the first and second currents vary substantially sub-exponentially.

34. (Rejected) A method according to claim 19 wherein the first and second currents vary substantially sub-exponentially.

35. (Rejected) A multiplier according to claim 21 wherein the first, second, third and fourth currents comprise substantially sub-exponential currents.

36. (Rejected) A method according to claim 24 wherein the first, second, third and fourth currents vary substantially sub-exponentially.

EVIDENCE APPENDIX

Copies of the following references are attached:

U.S. Patent No. 5,909,136 to Kimura ("Kimura") entered in the record through form PTO-892 as part of Paper No. 111204 mailed November 17, 2004.

U.S. Patent No. 6,173,346 to Wallach et al. ("Wallach") entered in the record through form PTO-892 as part of Paper No. 020406 mailed February 7, 2006.

The following table of values is based on Equation D in the Response to Final Office Action filed October 2, 2006 and was entered in the Advisory Action mailed October 19, 2006.

V_i / V_T	**Ic2 (for α_F = 0.98)**	**Ic2 (for α_F = 0.99)**	**Ic2 (for α_F = 1.0)**
0	1	1	1
0.25	0.782744	0.78077	0.778801
0.5	0.612877	0.609697	0.606531
0.75	0.480176	0.476261	0.472367
1	0.376581	0.372216	0.367879
1.25	0.29575	0.291111	0.286505
1.5	0.232707	0.2279	0.22313
1.75	0.183553	0.178643	0.173774
2	0.145238	0.140265	0.135335
2.25	0.115377	0.110366	0.105399
2.5	0.09211	0.087074	0.082085
2.75	0.073981	0.068931	0.063928
3	0.059858	0.054798	0.049787
3.25	0.048856	0.043791	0.038774

RELATED PROCEEDINGS APPENDIX

None.